20-GHz High-Efficiency AlInAs–GaInAs on InP Power HEMT

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Abstract—**A single stage 20-GHz power amplifier was developed using double-doped AlInAs–GaInAs on InP HEMT. Output power of 516 mW (0.645 W/mm) with power-added efficiency of 47.1% with 7.1-dB gain were obtained from an 800-μm wide device. The device had a saturated output power of more than 560 mW (0.7 W/mm). This is believed to be the highest combination of output power, power density, gain, and power-added efficiency reported for an InP-based FET at this frequency.**

I. Introduction

AlInAs–GaInAs on InP HEMT's are extensively used for microwave and millimeter wave low noise applications [1], [2]. The large conduction band discontinuity, high channel mobility, and high peak velocity in $Ga_{0.47}In_{0.53}As$ result in high transconductance, very low parasitic resistances, and excellent high-frequency performance. Due to the large conduction band discontinuity between $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}As$ high 2DEG density can be achieved in the channel of these HEMT's and combined with the high electron velocity of the channel high-current densities can be achieved. InP also has a higher thermal conductivity than GaAs allowing more dissipated power per unit chip area or lower channel operating temperature. Despite these advantages, little work has been done on AlInAs/GaInAs on InP HEMT's for power applications at microwave frequencies. This has been due to the two major drawbacks of these HEMT's of the low Schottky barrier height of metals on $Al_{0.48}In_{0.52}As$, and the low gate-to-drain breakdown voltage. We previously reported that by proper device layer design it is possible to overcome these drawbacks, and we reported output power densities of as high as 1 W/mm and power-added efficiencies of as high as 59% at 12 GHz [3]. The highest output power reported for an AlInAs–GaInAs–InP HEMT at 20 GHz has been 39 mW with power-added efficiency of 44%, and the maximum power-added efficiency of 52% with output power of 21 mW [4]. In this letter, we report on the power performance of an 800-μm wide AlInAs–GaInAs on InP HEMT at 20 GHz. The combination of output power, power density, gain, and efficiency for this device is comparable to the best reported performance of pseudomorphic GaAs-based HEMT's, and AlGaAs–GaAs HBT's at these frequencies [5]–[7].

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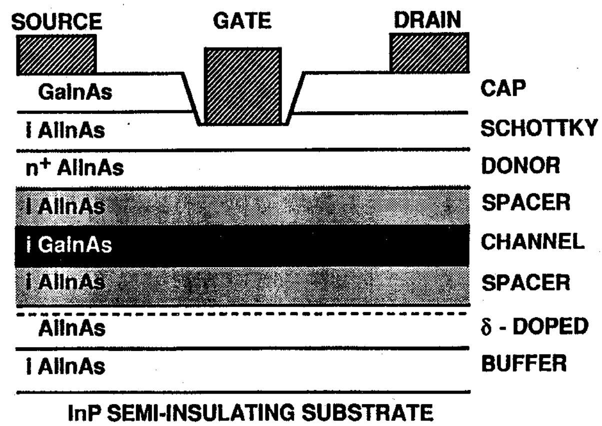

Fig. 1. Layer structure of the double-doped AlInAs–GaInAs on InP power HEMT.

II. Device Structure

The HEMT's were fabricated on a double-doped layer strucure shown in Fig. 1. The layers were grown by MBE lattice matched to a semi-insulating InP substrate. A double-doped layer structure is commonly used for power HEMT's to increase the sheet charge in the channel (2DEG density) to achieve high current densities, and to improve the gate-to-drain breakdown voltage by removing some of the donors from the top donor layer to the bottom donor layer. But double-doped device structures have not been widely utilized in AlInAs–GaInAs–InP material system because of the poor mobility of the two-dimensional electron gas (2DEG) formed at the inverted modulation-doped interface. The degraded characteristics of the inverted modulation-doped interface as compared with the normal (AlInAs on GaInAs), result from the surface segregation of silicon in AlInAs. When the inverted interface is modulation doped, silicon moves into the GaInAs channel, increasing the ionized impurity scattering of the 2DEG. By growing a thin layer of AlInAs immediately following the doped region at significantly reduced substrate temperatures (300 to 350° C) we have been able to reduce the silicon movement [8].

The layer structure used for the fabrication in this study had a δ-doped layer below the GaInAs channel (with a concentration of $2.0 \times 10^{12} cm^{-2}$) separated from the channel with a spacer layer thickness of 50 Å. The channel was 200-

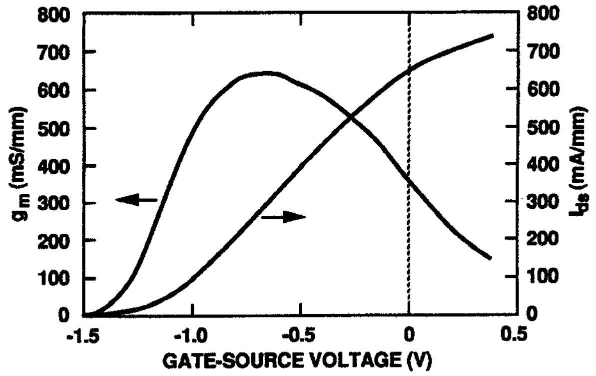

Fig. 2. Plot of transconductance and drain current as a function of gate-to-source bias at V_{ds}=1.5 V for a 0.2 μm × 300 μm AlInAs–GaInAs on InP HEMT.

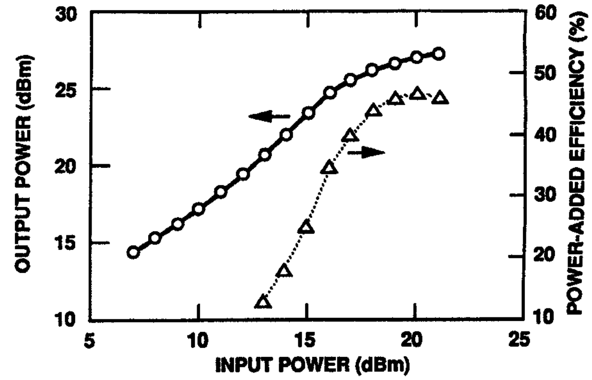

Fig. 3. Output power and power-added efficiency versus input power for an 800-μm wide HEMT at 20 GHz.

Å thick with an additional donor layer consisting of 50 Å of silicon doped AlInAs layer separated by a 25-Å spacer layer on top of the channel. The Schottky layer consists of 250 Å of undoped $Al_{0.70}In_{0.30}As$. The Schottky barrier height of Ti–Pt–Au on $Al_{0.48}In_{0.52}As$ can be substantially increased by adding more aluminum in the AlInAs Schottky layer [9]. The gate-to-drain turn-on voltage, as measured at 1 mA/mm of forward current, increased from 0.5 V to approximately 1.0 V by increasing the aluminum concentration from 48% to 70%. A 70-Å $Ga_{0.47}In_{0.53}As$ cap layer was used to facilitate ohmic contact formation to the material.

The material used for the fabrication of the power HEMT's had an electron sheet charge density of $4.5 \times 10^{12}\text{cm}^{-2}$ with a mobility of over 10 000 cm^2/V-s. The HEMT's were fabricated using a planar process. Source and drain ohmic contacts were formed using AuGe–Ni–Au alloy with drain-to-source spacing of 2 μm. Boron ion implantation was used for device isolation. The gates with a T-shaped cross-section and a footprint of 0.2 μm were formed by Ti–Pt–Au metallization. The HEMT's had a unit gate-finger width of 100 μm and a total gate-width of 800 μm with a gate-to-gate spacing of 20 μm. The completed wafer was lapped to a thickness of 100 μm before back metallization.

III. Device Performance

A plot of transconductance and drain current as a function of gate-to-source voltage for a typical 300-μm (4 × 75 μm) wide HEMT from the same wafer as the 800-μm wide devices tested is shown in Fig. 2. The characteristics were measured at a drain-to-source bias of 1.5 V. The transistor has a maximum transconductance of 630 mS/mm and a full channel current of 720 mA/mm measured at a gate bias of 0.4 V. Using double-doped layer structures with higher 2DEG densities we have been able to achieve full channel currents of more than 1000 mA/mm but in this case the maximum current was intentionally reduced (by using a material with a sheet charge density of $4.5 \times 10^{12}\text{cm}^{-2}$) to achieve lower power denisties, lower channel operating temperature, and more reliable operation. The device has a transconductance of more than 300 mS/mm across a drain current range of 37 to 630 mA/mm. A high transconductance over such a wide current range results in high-efficiency operation of the transistor. The gate-to-drain breakdown voltage of the transistor measured at 1 mA/mm of gate current was over 7 V. The transistors had a typical current gain cut-off frequency (f_T) of over 100 GHz. The 800-μm wide HEMT's were mounted in microstrip fixtures with a typical fixture loss of approximately 0.3 dB at 20 GHz. Source grounding was achieved using multiple gold wire-bonds. The transistors were biased for Class AB operation at a drain-to-source voltage of 4 V and a drain current of about 200 mA. The devices were then tuned by placing gold ribbons along the microstrip lines to optimize the performance of the amplifier. Plot of output power and power-added efficiency versus the input power for an 800-μm wide transistor is shown in Fig. 3. The device has a maximum power-added efficiency of 47.1% with an output power of 516 mW (0.645 W/mm) and gain of 7.1 dB. The linear gain of the transistor is approximately 8.5 dB with a saturated output power of over 560 mW (0.7 W/mm).

IV. Conclusion

State-of-the-art power performance of AlInAs–GaInAs on InP HEMT's has been achieved at 20 GHz. The combination of output power, power density, gain, and efficiency is comparable to the best results reported for AlGaAs–InGaAs on GaAs pseudomorphic HEMT's and AlGaAs–GaAs HBT's at this frequency. These results show the great potential for InP-based HEMT's for high-power and high-efficiency microwave applications.

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